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# Transistor Implementation Of Reversible Gate Using Novel 3 Transistor EX-OR Gate

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## Abstract

The design of VLSI systems with less power dissipation has become an area of intense research interest. The development for the design of such a low power systems undoubtedly requires the efficient designing methodology. Reversible Logics are one of the alternatives for removing the power dissipation problem in the VLSI systems at logical level implementation. In this regard, at the physical or circuit level transistor count is one of the important optimization issue in the VLSI design. This paper proposes an effective CMOS design of the main reversible logic gates of the reversible programmable logic array for the low power industrial application with less transistor count as explained in the literature. EX-OR is the main functionality of the reversible gates and in this paper the authors also shows the effective design of the EX-OR functionality by using 3 transistors.

**Keywords** – CMOS, Reversible Logics, EX-OR gate, Transistor Count.

## 1. INTRODUCTION

The advance laptop computers, digital cameras, processors, wearable computers, smart cards etc. are the witness of rapid growth of the semiconductor industries since the last decades. This rapid and explosive growth forces designer to struggle for the smaller silicon area, longer battery life and more reliability. So, the demands for the low power VLSI systems are also increasing for designing such hardware. According to the Gordon Moore (Co-founder of Intel) gave a rule of thumb, the number of transistors that can be placed inexpensively on an IC double approximately every two years. The hardware which are designed by conventional approach are irreversible hardwires. According to the Rolf Landauer in 1961, on a single bit of computation the heat produced by the conventional digital hardware is KTln2 [1]. Where K is a Boltzmann's constant equal to $1.3807\times10^{-23}JK^{-1}$ and T is the temperature at which the computation is performed.

At room i.e. 300k, this value becomes $2.8\times10^{-23}$J/Transistor approx [2]. This value is not to be negotiable for complex systems. Thus, an alternative approach comes in the existence known as reversible logic which does not dissipates heat as predicted by C.H. Benet in 1973. Reversible logics are the logics, in which the inputs can be retrieved by the outputs or in other words we can say that, if the logic runs backward known as reversible logics [2]. For a proper reversibility, the logic not only logically reversible but must also be physical reversible. For representation of N×N reversible gate for designing any reversible hardware, the number of inputs & outputs are N i.e.

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$$I_v = (I_1, I_2, I_3, \dots\dots\dots\dots\dots, I_N)$$
$$O_v = (O_1, O_2, O_3, \dots\dots\dots\dots\dots, O_N)$$

Where $I_v$ = input vectors
$O_v$ = output vectors
So, for reversibility, the numbers of inputs and outputs are same.

## 2. DESIGN METHODOLOGY OF HARDWARE

For designing any of the hardware, the designer follows number of steps which are shown in fig.1

| | |
|---|---|
| 1 | Algorithms |
| 2 | High Level Language |
| 3 | Machine Codes |
| 4 | Computer Architecture |
| 5 | Gate/ Logical Level Implementation |
| 6 | Circuit Level Implementation |

Fig. 1 Design Procedure of a digital hardware

The gate/ logical level designing are the design of blocks defined as the micro architecture at the logic gate levels. The last level is the circuit level implementation which is the transistor level design of the basic elements like gate, multiplexers etc.
So, in this paper the authors shows the transistor level/ circuit level implementation of the main logical blocks of the cost-effective reversible programmable logic array by effective structure of CMOS – XOR gate, which is implemented by only 3- transistor. The logical/ gate level implementation of the reversible programmable logic array has been already discussed by the authors in ref. 2

## 3. REVESIBLE LOGIC GATE

A logic gate 'G' is reversible if, for any output there is unique input 'A', such that applying G (A) = P. If a gate 'G' is reversible, there is an inverse gate G' which maps P to A. for which G (A) = P. So, a reversible gate inputs can be uniquely determined from its outputs. For logical reversibility in the digital logics there are two conditions as follows [2].

Fan-Out is not permitted
Feedback is not permitted

Some of the important and main measure in designing of the reversible logic circuits are QC (Quantum cost) [2]: The number of reversible gates (1×1 or 2×2) to realize the circuit is known as quantum cost, (CI) Constant inputs [2]: The number of inputs that are kept constant (0 or 1) for synthesis the given functions, GO (Garbage outputs) [2]: The number of outputs that are not primary is known as Garbage outputs

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There are several reversible logic gates in the literature like Feynman gate (FG), Toffolli gate (TG), Fredkin gate (FRG), Peres gate (PG), New gate (NG, MKG, HNG and TSG, MG) [2]. Here we are reviewing the, Feynman gate and MG (MUX gate) [2] because these gates are the basic gates of the destined structure.

*A.* Feynman Gate

Fig.2 shows the 2×2 reversible gate called Feynman gate. Feynman gate is also recognized as controlled- not gate (CNOT). It has two inputs (A, B) and two outputs (P, Q). The outputs are defined by P=A, Q=A XOR B .This gate can be used to copy a signal. Since fan-out is not allowed in reversible logic circuits, the Feynman gate is used as the fan-out gate to copy a signal. Quantum cost of a Feynman gate is 1.

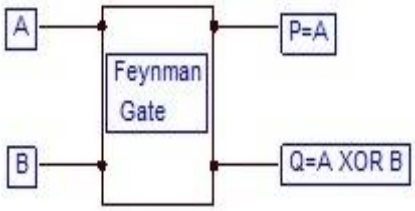


Fig.2: 2×2Feynman gate structure

*B.* MUX Gate

Fig.3 shows the pictorial representation of 3×3 reversible gate called MUX (MG) gate [2]. It is a conservative gate having three inputs (A, B, C) and three outputs (P, Q, R). The outputs are defined by P=A, Q=A XOR B XOR C and R= A'C XOR AB. The hamming weight of its input vector is same as the hamming weight of its output vector and its Quantum cost is 4.

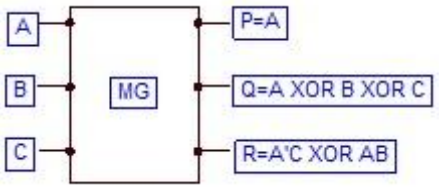


Fig.3: 3×3 MUX gate

## 4. CMOS REALIZTION OF REVERSIBLE GATES

The effective design of the 3- Transistor EX-OR gate is shown in fig.4. Which is the modified design of CMOS inverter and a PMOS pass transistor? In this design [3], when the input B is at logic 1 or high, the left portion of the circuits acts as a normal CMOS inverter. Therefore the output Y is complementary of the input A. When the input B is at logic 0 or low, the CMOS inverter output is at high impedance and the pass transistor T3 is enabled and the output Y will be the same logic value as input A[5].

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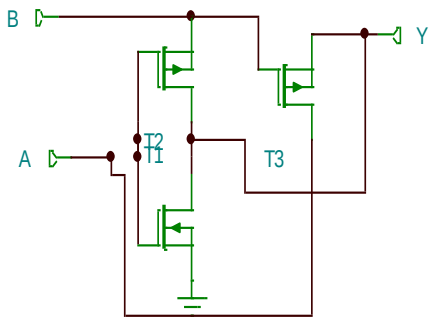


Fig. 4 3-Transistor CMOS Realization of EX-OR gate

Working table of New CMOS EX-OR gate

| Input A | Input B | T1 | T2 | T3 | Output |
|---|---|---|---|---|---|
| Low | Low | ON | OFF | OFF | Low |
| Low | High | ON | OFF | OFF | High |
| High | Low | OFF | ON | ON | High (Degraded) |
| High | High | OFF | OFF | OFF | Low |

However when A=1 and B=0, there is a voltage degradation due to threshold drop across transistor T3 resultantly the output Y will also degraded wart input. This degradation can be minimized by increasing the W/L ratio of the T3 [3] because

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + \emptyset_0} - \sqrt{\emptyset_0}\right) - \alpha_l \frac{t_{ox}}{L}(V_{SB} + \emptyset_0) - \alpha_v \frac{t_{ox}}{L}(V_{DS}) + \alpha_w \frac{t_{ox}}{W}(V_{SB} + \emptyset_0) \quad \ldots\ldots\ldots (1)$$

Where $V_{T0}$ is the zero bias threshold voltage, $\gamma$ is the bulk threshold coefficient, $\emptyset_0$ is $2\emptyset_F$, where $\emptyset_F$ is the Fermi potential, $t_{ox}$ is the thickness of the oxide layer and $\alpha_l$ , $\alpha_v$ , $\alpha_W$ are the process dependent parameters. So, from eq (1) it is clear that by increasing the W it is possible to decrease the threshold voltage and therefore by increasing the width of transistor T3, keeping the length constant, it is possible to
Minimize the voltage degradation due to threshold voltage drop [3].

*A.* Transistor Implementation of Feynman Gate & MUX gate

The transistor level implementation of the Feynman gate and the MUX gate is shown in fig. 5 & fig.6. This implementation uses the novel 3- transistor xor gate structure to make the circuit less complex and also having less delay due to the less critical paths. The AND structure of CMOS transistor s same as we studied in the literatures.

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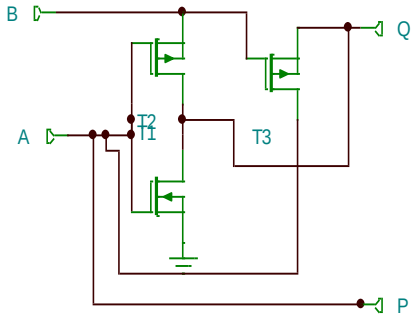


Fig.5 Transistor Implementation of Feynman Gate by 3-Transistor EX-OR gate

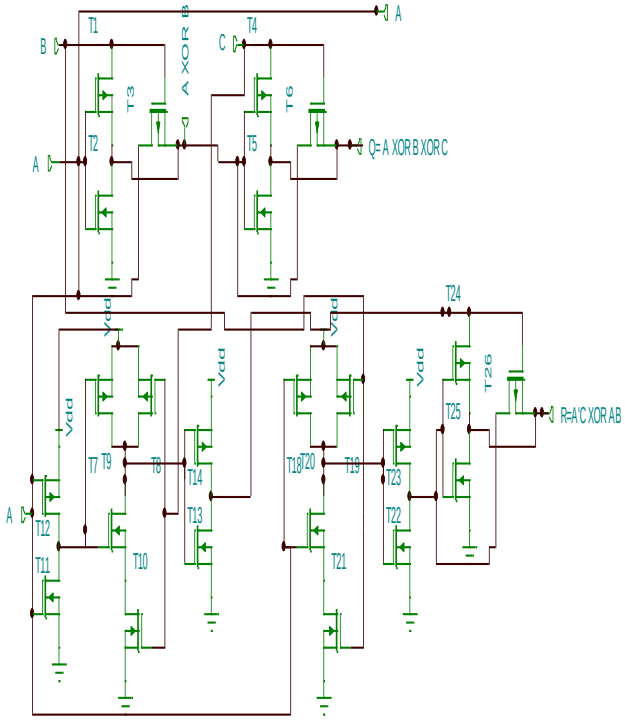


Fig. 6 Transistor Implementation of MUX Gate by 3- Transistor EX-OR gate

## 5. RESULT & DISCUSSION

The CMOS realization of the main logic blocks of the reversible programmable logic array has been proposed. This work proposes the effective design of CMOS MUX gate & CMOS Feynman gate by using novel 3 transistor based EX-OR gate. The transistor count in the proposed design is less than the existing design methodology [4]. In the proposed design of current work the numbers of transistors used are 3 for Feynman gate & 23 for MUX gate. However the existing approach provides 4 transistors for Feynman gate & 26 for MUX gate can be seen in the table 2.

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Table 2 Comparison of Two Design Methodologies

| Reversible Gate | No. Of Transistor used | |
|---|---|---|
| | Propose | Existing[4] |
| Feynman gate | 3 | 4 |
| MUX gate | 23 | 26 |

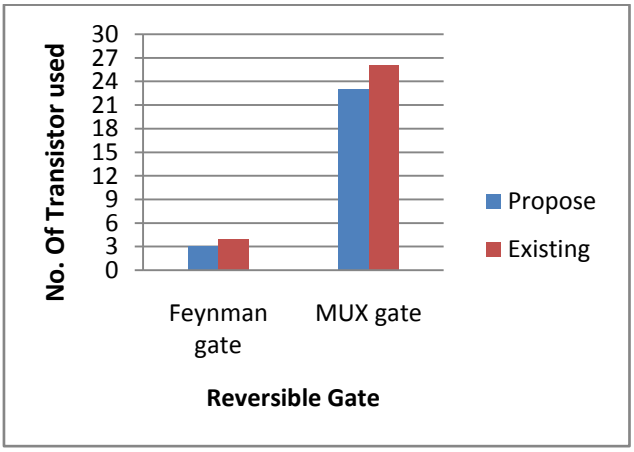


Fig. 7 Comparison of Proposed & Existing Design

As we can see the results in the table, the number of transistor used in the reversible gates are less as compare to the existing design. So, this proposed structure of Novel 3- transistor XOR gate is better for realizations of reversible circuits at circuit level implementation for the low power industrial applications.

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